REMARKS

Claims 80, 84, and 93 are amended. Claims 1-79 have been cancelled without prejudice. New claims 97-106 are added. The office action indicates that it is responsive to the Applicant's communication filed on September 15, 2003 (the actual filing date of the Application); however, Applicant understands that it is actually responsive to the preliminary amendment filed by the Applicant on May 2, 2007, which added the claims addressed in the office action.

The Examiner has indicated by striking-through that several references cited in the Information Disclosure Statement have not been considered. The office action is not clear on why the stricken-through references have not been considered – Applicant respectfully requests an explanation.

Claims 80 and 84 stand objected-to for informalities. In view of the amendment to these claims, Applicant respectfully requests that the objection be withdrawn.

Claims 80, 81, 83-85, 87-89 and 91 stand rejected under the judicially created theory of obviousness-type double patenting as being unpatentable over claims 14, 18, 21, 33, 35, and 37 of U.S. Patent 6,654,057 ("the '057 patent"). In view of the terminal disclaimer file herewith, this objection is respectfully requested to be withdrawn.

Claims 80-83 and 88-96 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,721,422 ("Bird"). Applicant respectfully traverses this rejection.

Claim 80 defines a method of operating an active pixel CMOS imager and recites "activating a first pixel in a row of pixels connected to a shared column line and then subsequently activating an adjacent second pixel in the row of pixels connected to the shared column line, the first and second pixels disposed in a pixel array;" and "resetting a voltage level of a node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;" and "transferring charge collected by the first pixel to the node;"

and "detecting the charge at the node;" and "generating an output signal over the shared column line corresponding to the charge detected at the node." Such a method is not disclosed by Bird.

Bird does not disclose "resetting a voltage level of a node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array," as recited by independent claim 80. Bird does not have a designated "reset line" and the lines it indicates are used for resetting, i.e., reference lines (1 and 2 – *see* FIG. 1 and col. 6, ll. 24-28 and 45-49), travel circuitously across the array, not approximately linearly, as shown in FIG. 1 from Bird, reproduced below:

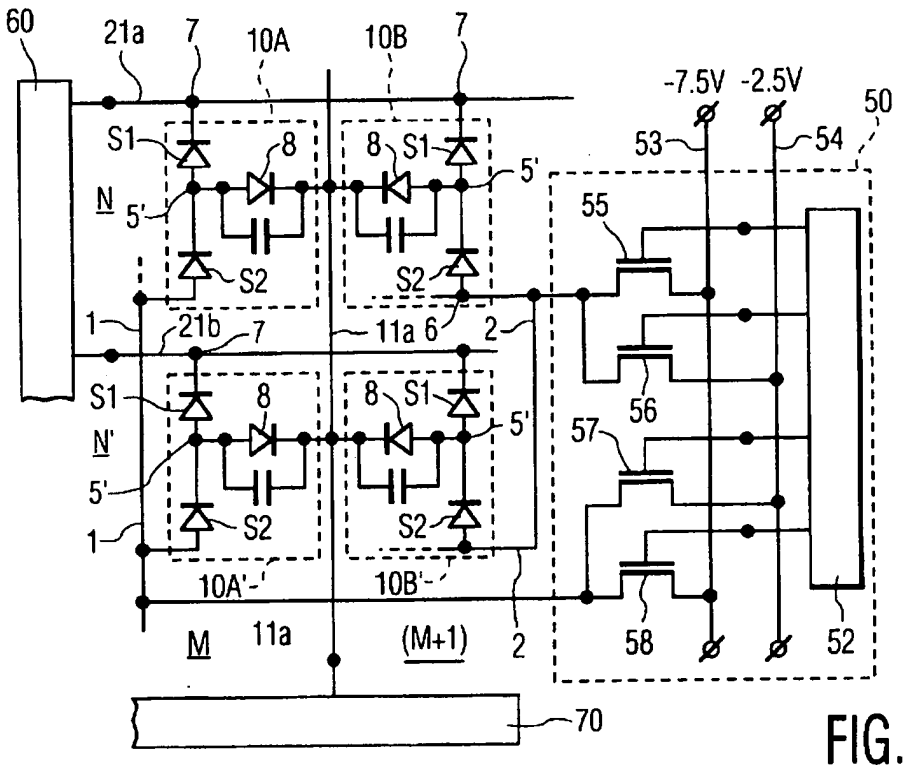

FIG. 1

Since Bird fails to disclose each limitation of independent claim 80 and claims 81-83 depend from independent claim 80, Bird does not anticipate these claims and the 35 U.S.C. § 102(b) rejection thereof is respectfully requested to be withdrawn.

Claim 88 defines an active pixel CMOS imager and recites "a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array;" and "a plurality of column lines each connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal;" and "a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows;" and "a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows;" and "a column driver to address pixels connected to the column lines;" and "a row driver to address pixels through the odd row select lines and the even row select lines." This apparatus is not disclosed by Bird.

Bird does not disclose "a plurality of odd row select lines . . . to address odd pixels in the rows" or "a plurality of even row select lines . . . to address even pixels in the rows" or "a row driver to address pixels through the odd row select lines and the even row select lines." Bird uses single row lines (i.e. 21a) for all pixels (i.e., 10A and 10B) in a row (i.e., N) and relies on a secondary set of additional lines (i.e., 1 and 2), called "reference conductors" to segregate signals to adjacent pixels on a same column line. This can be clearly seen in Bird's FIG. 1, which is reproduced above in the discussion of the patentability of claim 80. Thus, Bird's device is not the same as that defined by independent claim 88.

Since Bird fails to disclose each limitation of independent claim 88 and claims 89-92 depend from independent claim 88, Bird does not anticipate these claims and the 35 U.S.C. § 102(b) rejection thereof is respectfully requested to be withdrawn.

Claim 93 defines a method of operating a CMOS imager and recites "addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line;" and "providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; and "addressing odd pixels in the row of pixels via an odd row select line;" and "providing a second output signal associated with light detected by the odd pixels to the plurality of column lines coupled to the odd pixels." This method is not disclosed by Bird.

None of the limitations relating to the presence and use of even and odd row lines, particularly as they are connected to a row driver, are disclosed by Bird. In this context, Bird fails to disclose "addressing even pixels in a row of pixels of an array of pixels" and "using a row driver coupled to an even row select line" and "providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels" and "addressing odd pixels in the row of pixels via an odd row select line" and "providing a second output signal associated with light detected by the odd pixels to the plurality of column lines coupled to the odd pixels." As discussed above in relation to the patentability of independent claim 88, Bird's device uses single row lines (i.e. 21a) for all pixels (i.e., 10A and 10B) in a row (i.e., N) and relies on a secondary set of additional lines (i.e., 1 and 2), called "reference conductors" to segregate signals to adjacent pixels on a same column line. Thus, Bird's device and the methods of using it are different from what is defined by claim 93.

Since Bird fails to disclose each limitation of independent claim 93 and claims 94-96 depend from independent claim 93, Bird does not anticipate these claims and the 35 U.S.C. § 102(b) rejection thereof is respectfully requested to be withdrawn.

Claim 84 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Bird in view of U.S. Patent 5,576,763 ("Ackland et al."). Applicant respectfully traverses this rejection. Although the office action is vague on whether claims 85-87 are likewise rejected over these same references along with claim 84, for the purposes of this response Applicant will assume that they are so rejected and respectfully traverses such rejection.

Claim 84 defines a method of operating a system and recites "focusing an image on an active pixel CMOS imager, the imager comprising a pixel array;" and "activating a first pixel in a row connected to a shared column line and then subsequently activating an adjacent second pixel in the row connected to the shared column line, the pixel array comprising the first and second pixels;" and "resetting a voltage level of a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;" and "transferring charge collected by the first pixel to the node;" and "detecting the charge

at the node" and "generating an output signal over the shared column line, the output signal corresponding to the image." This method is not taught or suggested by Bird and Ackland, whether the two are taken individually or in combination.

As discussed above regarding the patentability of claim 80 over Bird, the references fails to disclose "using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array," as similarly recited by claim 84 since Bird does not have a designated "reset line" and the lines it indicates are used for resetting, i.e., reference lines (1 and 2 – *see* FIG. 1 and col. 6, ll. 24-28 and 45-49), travel circuitously across the array, not approximately linearly, as shown in FIG. 1 from Bird (reproduced above). Ackland is cited in the office action only for its disclosure of focusing an image on a pixel. Even if Ackland does disclose such a feature, it does not remedy the lack of disclosure in Bird to teach or suggest the claimed method.

Since Bird and Ackland fail to disclose, teach or suggest each limitation of independent claim 84 and claims 85-87 depend from independent claim 84, these claims would not have been obvious over Bird and Ackland and the 35 U.S.C. § 103(a) rejection thereof is respectfully requested to be withdrawn.

Applicant believes the pending application is in condition for allowance and respectfully requests that it be passed to issue.

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Respectfully submitted,

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